

## 20V N-Ch Power MOSFET

### Feature

- ◇ High Speed Power Switching, Logic Level
- ◇ Enhanced Avalanche Ruggedness
- ◇ Lead Free, Halogen Free

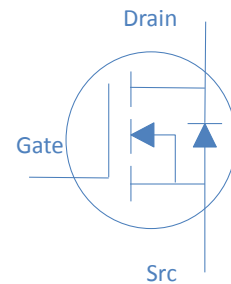
$V_{DS}$		20	V
$R_{DS(on),typ}$	$V_{GS}=4.5V$	13	mΩ
$I_D$ (Silicon Limited)		8	A

### Application

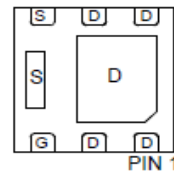
- ◇ Hard Switching and High Speed Circuit
- ◇ DC/DC in Telecoms and Industrial

Part Number	Package	Marking
HTL140N02	DFN2*2	1L

DFN2\*2



Bottom View



### Absolute Maximum Ratings at $T_J=25^\circ\text{C}$ (unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	$I_D$	$T_C=25^\circ\text{C}$	8	A
		$T_C=70^\circ\text{C}$	6.2	
Drain to Source Voltage	$V_{DS}$	-	20	V
Gate to Source Voltage	$V_{GS}$	-	$\pm 12$	V
Pulsed Drain Current	$I_{DM}$	-	32	A
Avalanche Energy, Single Pulse	$E_{AS}$	$L=0.1\text{mH}, T_C=25^\circ\text{C}$	5.0	mJ
Power Dissipation	$P_D$	$T_C=25^\circ\text{C}$	2.08	W
Operating and Storage Temperature	$T_J, T_{stg}$	-	-55 to 150	$^\circ\text{C}$

### Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	60	$^\circ\text{C/W}$
Thermal Resistance Junction-Case	$R_{\theta JC}$	12	$^\circ\text{C/W}$

**Electrical Characteristics at  $T_J=25^{\circ}\text{C}$  (unless otherwise specified)**
**Static Characteristics**

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	20	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	0.4	0.75	1.2	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS}=0V, V_{DS}=16V, T_J=25^{\circ}\text{C}$	-	-	1	$\mu A$
		$V_{GS}=0V, V_{DS}=16V, T_J=125^{\circ}\text{C}$	-	-	10	
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS}=\pm 12V, V_{DS}=0V$	-	-	$\pm 100$	nA
Drain to Source on Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=8A$	-	13	14.8	m $\Omega$
		$V_{GS}=2.5V, I_D=5A$	-	19	23	
Transconductance	$g_{fs}$	$V_{DS}=5V, I_D=8A$	-	9	-	S

**Dynamic Characteristics**

Input Capacitance	$C_{iss}$	$V_{GS}=0V, V_{DS}=10V, f=1\text{MHz}$	-	1192	-	pF
Output Capacitance	$C_{oss}$		-	203	-	
Reverse Transfer Capacitance	$C_{rss}$		-	174	-	
Total Gate Charge	$Q_g(10V)$	$V_{DD}=10V, I_D=8A, V_{GS}=4.5V$	-	14.2	-	nC
Gate to Source Charge	$Q_{gs}$		-	1.8	-	
Gate to Drain (Miller) Charge	$Q_{gd}$		-	5.0	-	
Turn on Delay Time	$t_{d(on)}$	$V_{DD}=10V, I_D=1A, V_{GS}=4.5V, R_G=6\Omega,$	-	15	-	ns
Rise time	$t_r$		-	18	-	
Turn off Delay Time	$t_{d(off)}$		-	35	-	
Fall Time	$t_f$		-	20	-	

**Reverse Diode Characteristics**

Diode Forward Voltage	$V_{SD}$	$V_{GS}=0V, I_F=8A$	-		1.2	V
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Fig 1. Typical Output Characteristics

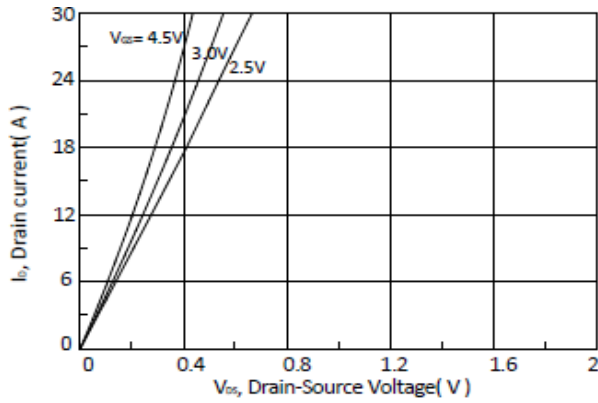


Figure 2. On-Resistance vs. Gate-Source Voltage

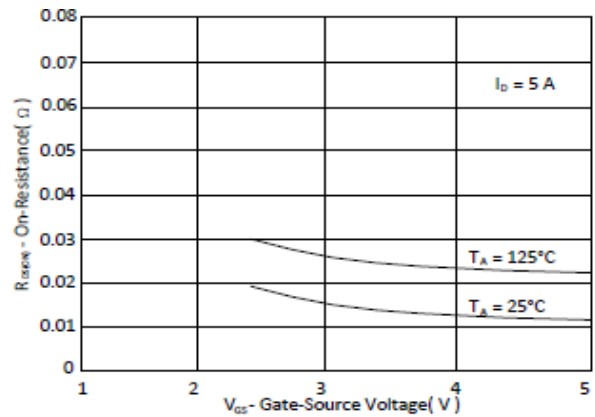


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

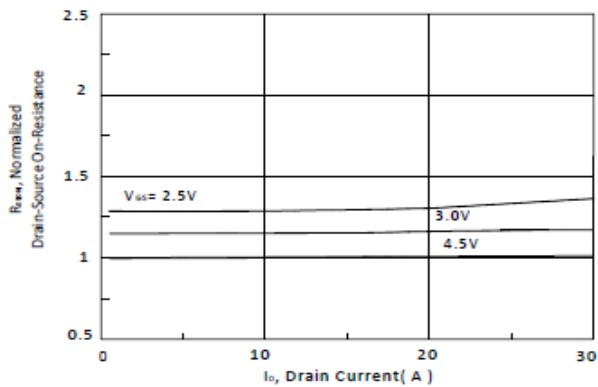


Figure 4. Normalized On-Resistance vs. Junction Temperature

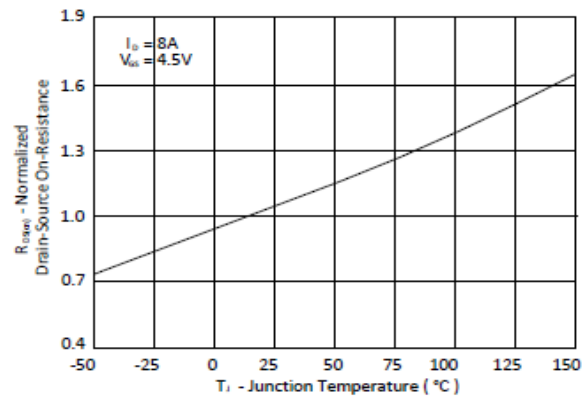


Figure 5. Typical Transfer Characteristics

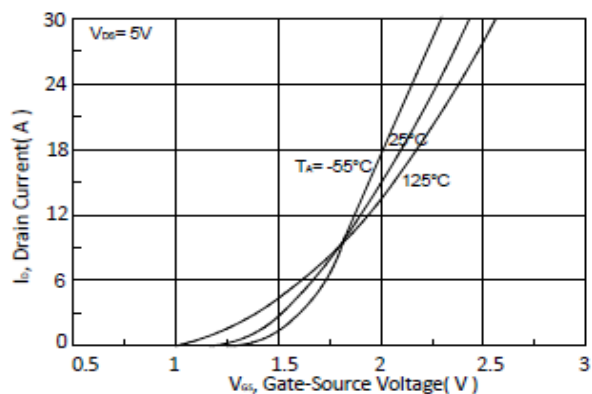


Figure 6. Typical Source-Drain Diode Forward Voltage

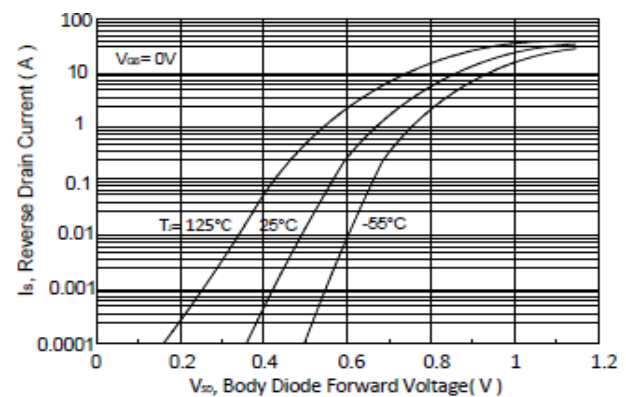


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

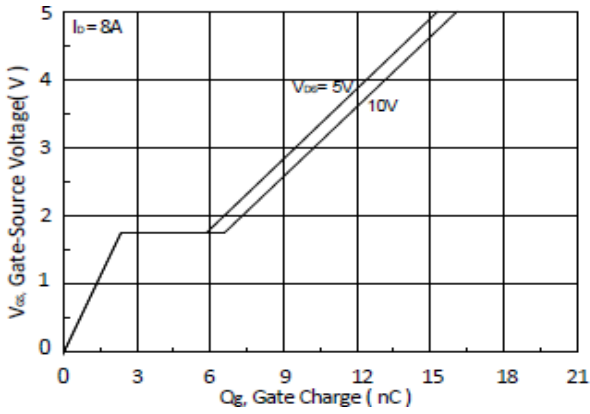


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

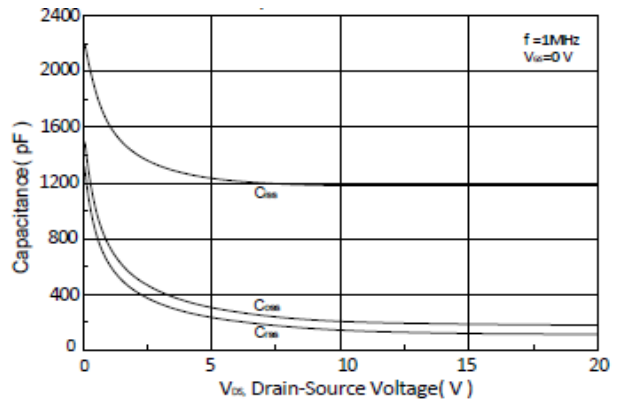


Figure 9. Maximum Safe Operating Area

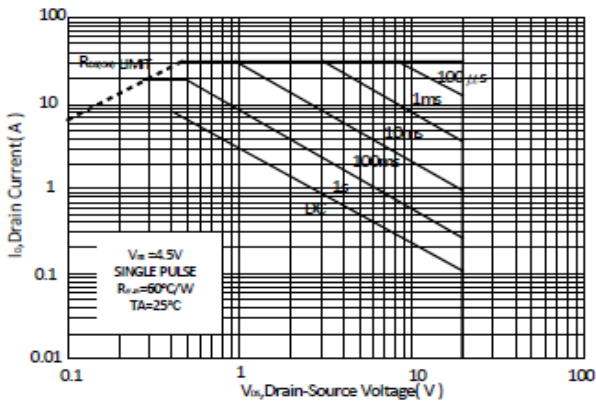


Figure 10. Single Pulse Maximum Power Dissipation

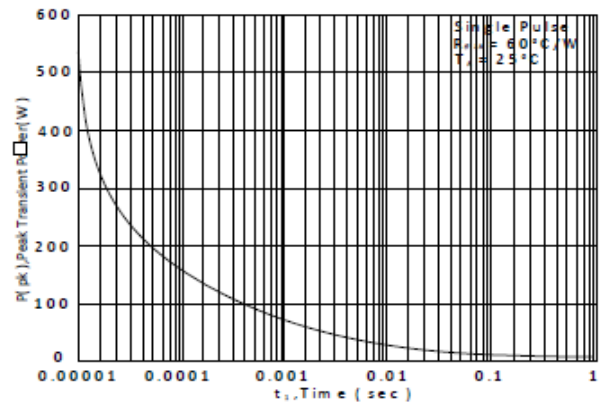
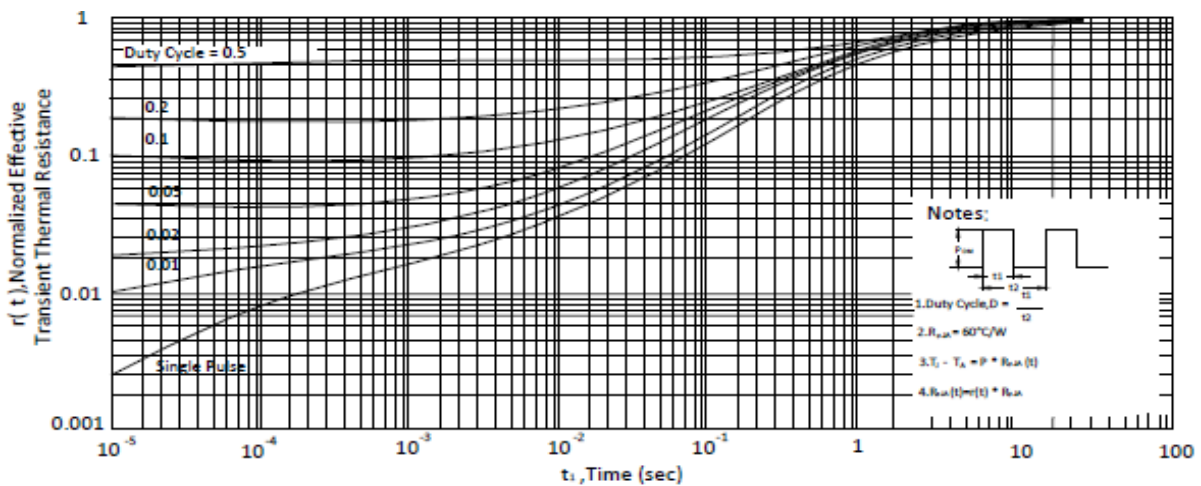
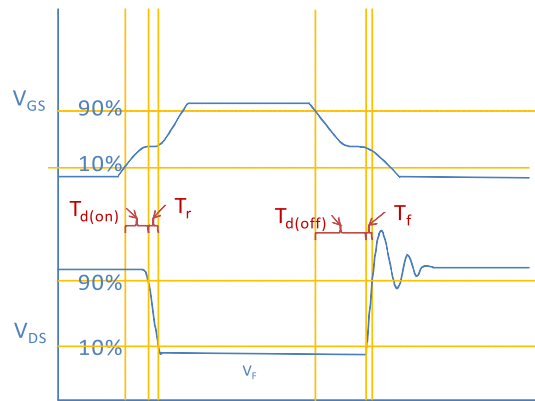
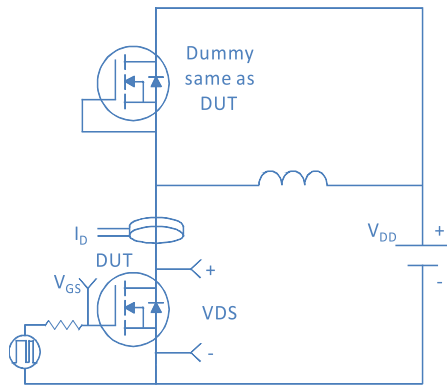


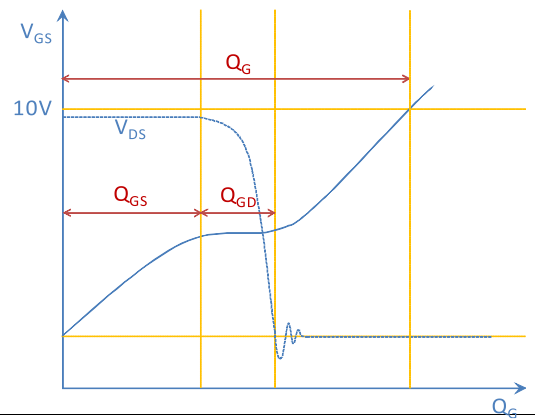
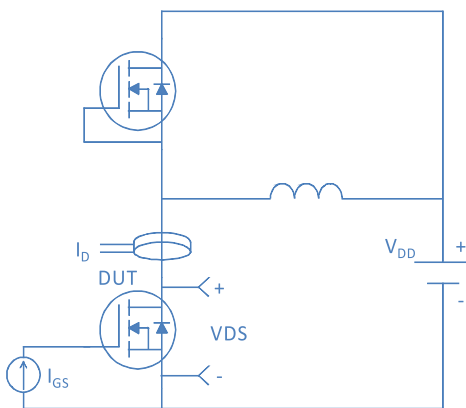
Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient



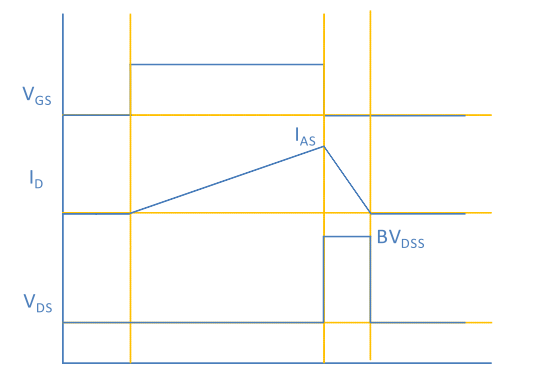
### Inductive switching Test



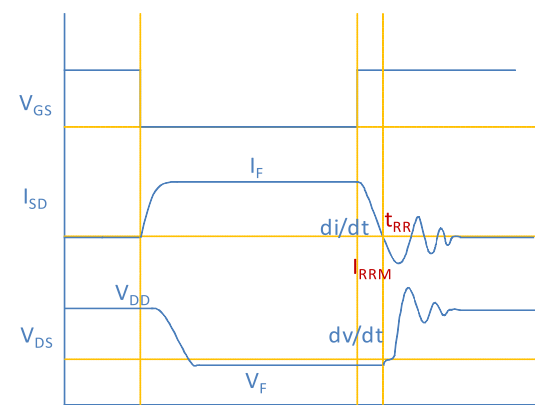
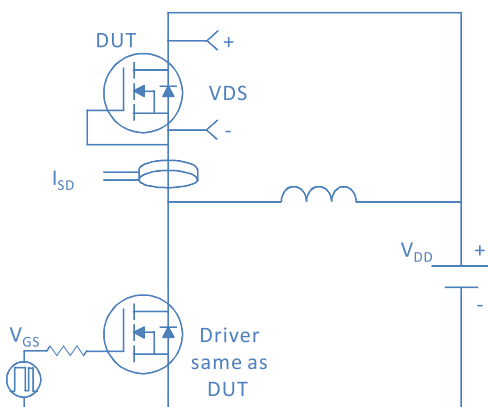
### Gate Charge Test



### Uclamped Inductive Switching (UIS) Test

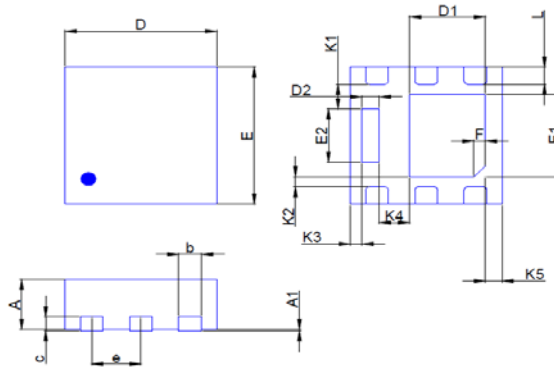


### Diode Recovery Test



Package Outline

DFN2\*2\_P, 6leads



Dimension in mm

Dimension	A	A1	b	c	D	D1	D2	E	E1	E2	e	F	f	K1	K2	L	K3	K4	K5
Min.	0.50	0.00	0.25		1.9	1.0	0.13	1.9	1.1	0.65				0.306	0.10	0.2	0.10	0.27	0.17
Typ.		0.02	0.30	0.1	2.0	1.1	0.25	2.0	1.2	0.75	0.65	0.15	45°	0.356	0.15	0.25	0.15		0.22
Max.	0.65	0.05	0.35		2.1	1.2	0.35	2.1	1.3	0.88				0.406	0.20	0.3	0.20		0.27

Recommended minimum pads

